We claim:

1. A power switch, comprising:

a controllable transistor having a load path and a control electrode;

a limiting transistor for limiting a voltage drop across said load path of said first transistor, said limiting transistor having a load path connected in series with said load path of said first transistor, and having a control electrode; and

an auxiliary transistor having a load path connected between said control electrode of said limiting transistor and a reference node, and having a control electrode connected between said first transistor and said limiting transistor.

2. The power switch according to claim 1, wherein said limiting transistor is a first limiting transistor and said auxiliary transistor is a first auxiliary transistor, and at least one second limiting transistor has a load path connected in series with said load path of said first limiting transistor, and at least one second auxiliary transistor has a load path connected between said control electrode of said first limiting transistor and said control electrode of said second limiting transistor, and a control electrode connected

between said load paths of said first and second limiting transistors.

3. The power switch according to claim 1, wherein said load path of said controlled transistor is connected between said limiting transistor and said reference node.

4. The power switch according to claim 1, which further comprises a power switch control terminal connected to said control electrode of said controllable transistor.

5. The power switch according to claim 1, wherein said limiting transistor has a source electrode and a gate electrode, and a Zener diode is connected between said source electrode and said gate electrode of said limiting transistor.

6. The power switch according to claim 2, wherein each of said first and at least one second limiting transistors has a source electrode and a gate electrode, and a Zener diode is connected between said source electrode and said gate electrode of each said limiting transistor.

7. The power switch according to claim 1, which comprises a Zener diode connected in parallel with said load path of said auxiliary transistor.

8. The power switch according to claim 2, which comprises Zener diodes connected in parallel with said load paths of each said auxiliary transistor.

9. The power switch according to claim 1, wherein said controllable transistor is a MOSFET of a first conductivity type, said limiting transistor is a normally on field-effect transistor of the first conductivity type, and said auxiliary transistor is a normally on field-effect transistor of a second conductivity type.

10. The power switch according to claim 2, wherein said controllable transistor is a MOSFET of a first conductivity type, said first and second limiting transistors are normally on field-effect transistors of the first conductivity type, and said first and second auxiliary transistors are normally on field-effect transistors of a second conductivity type.

11. The power switch according to claim 1, wherein said controllable transistor, said limiting transistor, and said auxiliary transistor are integrated in a semiconductor body.

12. The power switch according to claim 1, wherein said controllable transistor, said first and second limiting transistors, and said first and second auxiliary transistors are integrated in a semiconductor body.

13. A semiconductor configuration, comprising:

a semiconductor body and a power switch formed in said semiconductor body and having a load path running vertically through said semiconductor body;

said semiconductor body being formed with:

a substrate doped with charge carriers of a first conductivity type;

at least one well doped with charge carriers of a second conductivity type, and a MOSFET formed in said at least one well;

a first region formed in said substrate spaced apart from said well and heavily doped with charge carriers of the first conductivity type; and

a second region horizontally spaced apart from said first region and heavily doped with charge carriers of a second conductivity type.

14. The semiconductor body according to claim 13, wherein said first region is one of a plurality of first regions formed in said semiconductor body and spaced apart from one another in the vertical direction, and said second region is

one of a plurality of second regions formed in said semiconductor body and spaced apart from one another in the vertical direction.

15. The semiconductor body according to claim 14, which comprises interconnects connecting respectively adjacent second regions, said interconnects being formed by doping with charge carriers of the second conductivity type, and wherein said well is connected to one of said second regions by an interconnect.